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10/719,724	11/21/2003	Thomas J. Gilg	200308974-1	3164

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EXAMINER	
ABEDIN, SHANTO	

ART UNIT	PAPER NUMBER
2436	

NOTIFICATION DATE	DELIVERY MODE
12/18/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/719,724	GILG, THOMAS J.	
	Examiner	Art Unit	
	SHANTO M. ABEDIN	2436	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19,23 and 29-47* is/are pending in the application.

4a) Of the above claim(s) *1-8 and 17-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-16,23 and 29-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/06/2008 has been entered.

2. Claims 9-16, 23 and 29-47 have been presented for examination.

3. Claims 9-16, 23 and 29-47 have been rejected.

Response to Arguments

4. The applicant's arguments regarding the previous 35 USC 102 (e) type rejections are fully considered, however, found not persuasive. In particular, upon further consideration, reference Hayashi was found to teach the limitations set forth by the amended claims (please see below for further explanations). Although the examiner believes that the reference Hayashi sufficiently teaches, or suggests enablement of the claimed invention, the examiner incorporates a newly found reference Evans et al which further teaches the limitations set forth by the applicant's arguments. Therefore, the applicant's arguments are also moot in view of new grounds of rejection presented in this office action.

5. The applicant's arguments regarding previous 35 USC 112 first paragraph type rejections are fully considered. The previous 35 USC 112 first paragraph type rejections are withdrawn because of the amendments made to the claims.

6. The applicant's arguments regarding previous 35 USC 101 type rejections are fully considered, however, found not persuasive. In particular, invention set forth by the newly

amended claims 9-16 is considered to be non-statutory, and therefore, the previous 35 USC 101 type rejections of claims 9-16 are maintained. The examiner notes, upon further examination, new grounds of 35 USC 101 type rejections are found, and presented in this office action.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 9-16, 23, 29-40 and 43-46 are rejected under 35 USC 101 as the claimed invention is directed to non-statutory subject matter.

Regarding claims 9-16 and 23, they are directed to a device comprising the elements such as "pixel elements", "decryption logic", or "pixel logic", however, claim languages fail to disclose expressly any associated computer structure, or hardware elements - therefore, device elements such 'pixels', or 'logic' could be just software implemented data structure, or program only! Furthermore, according to the abstract and specification (especially Par 002 and 0011), these components are, or at least can be implemented in software only, and therefore being considered to be non-statutory. See MPEP 2106.01 [R-5].

Regarding claims 29-40 and 43-46, they are directed to system/ device comprising the elements such as source/ receiving 'pixels', encryption/ decryption 'logic', however, claim languages fail to disclose expressly any associated computer structure, or hardware elements. Although the claim limitations recite 'device', the actual components of such device fail to incorporate any hardware element. Therefore, device elements such 'pixels', or 'logic' could be just software implemented data structure, or program only! Furthermore, according to the abstract and specification (especially Par 002, 011 and 018), these components such as pixel

logic, encryption/decryption logic can be implemented in software only, and therefore being considered to be non-statutory. See MPEP 2106.01 [R-5].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 9-16, 23 and 29-47 are rejected under 35 U.S.C. 102(e) as anticipated by Hayashi (US 2004/0081334 A1) or, in the alternative, under 35 U.S.C. 103(a) as obvious over Evans et al (US 7,206,940 B2)

Regarding claim 9, Hayashi teaches a digital picture display device comprising:

a plurality of pixel elements arranged in an array (Fig 2A, 3A; Par 003, 049, 054-055; pixels/ image elements in array) and each configured to illuminate to form a picture in response to a digital data stream representing picture information (Par 003, 130, 158, 162; outputting/ reproducing, illuminating the image); and

decryption logic configured to receive an encrypted data stream from a source device and to decrypt picture information from the encrypted data stream for at least a first portion of the plurality of pixel elements with a first decryption key (Fig 14; Par 003-006, 129, 143-150; decryption key respective to image tiles/ pixels) and to decrypt picture information for at least a second portion of the plurality of pixel elements with a second decryption key (Par 003-006, 129, 143-150; plurality of decryption keys respective to each image tile/ pixel).

Alternatively, if the position of inherency is not found to be supportable, the examiner holds the position that it would have been obvious to a person with ordinary skill in the art to modify the Hayashi 's device by adding/ substituting Evans et al' s teachings of decrypting picture information from the encrypted data stream for at least a first portion of the plurality of pixel elements with a first decryption key and at least a second portion of the plurality of pixel elements with a second decryption key (Fig 11; Col 16, starts at line 10; per pixel decryption logic, key).

Evans et al and Hayashi are analogous art because they are from the same field of endeavor of secure image processing. At the time of invention, it would have been obvious to a person with ordinary skill in the art to combine/ substitute the teaching of Evans et al with Hayashi to design a device further comprising the plurality of keys for encrypting/ decrypting the plurality of pixels in order to provide a stronger pixel level data security.

Regarding claim 10, Hayashi teaches the digital picture display device according to claim 9, wherein: the first portion is a first single pixel element; and the second portion is a second single pixel element (Fig 3A, 3B; Par 003, 044, 054-061, 067; pixel/ tile groups) ; wherein the decryption device is adapted to decrypt picture information for each of the pixel elements with a different decryption key (Par 005-006, 040, 144-150; each pixel/ tile group associated with a different key).

Regarding claim 11, Hayashi teaches the digital picture display device wherein: each of the pixel elements includes decryption logic that connects to a respective one of the pixels (Par 124, 129, 135, 143-150; each pixel/ tile associated with specific decryption process, key).

Regarding claim 13, Hayashi teaches the digital picture display device wherein the first portion is a first plurality of pixels and the second portion is a second plurality of pixels (Par 006-008, 015, 143, 150; pixel/ tile grouping).

Regarding claim 14, Hayashi teaches the digital picture display device wherein the decryption device is a single component that decrypts the first portion with the first decryption key and decrypts the second portion with the second decryption key (Par 006-008, 127-130, 143, 150; respective pixel decryption keys)

Regarding claim 15, Hayashi teaches the digital picture display device further comprising: pixel logic adapted to receive decrypted picture information for the first portion from the decryption device and to receive decrypted picture information for the second portion from the decryption device and to dispatch the picture information for the first portion of pixel elements to the decryption device and to dispatch the picture information for the second portion to the second portion of pixel elements to the decryption device (Fig 11; Par 127-130, 139, 143, 149-150; decryption processing section receiving, outputting decryption logic/ information)

Regarding claim 16, Hayashi teaches the digital picture display device wherein the array is a picture gathering device of a digital camera (Par 006-008, 141-143; camera).

Regarding claim 23, it is rejected applying as same motivation applied rejecting claim 9, furthermore, Hayashi teaches a micro electronic device, comprising: an array of display pixels collectively configured to display visible images (Fig 2A, 3A; Par 003, 049, 054-058, 158, 162; pixels/ image elements in array; outputting/ reproducing, illuminating the image); and a

plurality of decryption logic components, each decryption logic component associated with different group of the display pixels and configured to decrypt video data directed to the respective group of display pixels (Par 003-006, 129, 143-150; plurality of decryption keys respective to each image tile/ pixel).

Alternatively, if the position of inherency is not found to be supportable, the examiner holds the position that it would have been obvious to a person with ordinary skill in the art to modify the Hayashi 's device by adding/ substituting Evans et al' s teachings of each decryption logic component associated with different group of the display pixels and configured to decrypt video data directed to the respective group of display pixels (Col 16, starts at line 10).

Regarding claim 29 and 47, they are rejected applying as same motivation applied rejecting claim 9, furthermore, Hayashi teaches a system/ method, comprising:

a source device including: a plurality of source pixels arranged into a plurality of regions, each region having at least one source pixel configured to capture digital picture information (Fig 2A, 3B; Par 003, 049, 054-058; pixels/ image elements in array; storing, receiving the image information) ; and

encryption logic configured to encrypt the captured digital picture information in at least one of the regions using a plurality of encryption keys (Fig 14; Par 006, 015, 040, 044, 150; encryption of the digital image using plurality of keys);

a receiving device in communication with the source device, the receiving device including: a plurality of receiving pixels configured to illuminate to form a picture in response to the digital picture information (Fig 2A, 3B; Par 003, 049, 054-058, 158, 162; pixels/ image elements in array; outputting/ reproducing, illuminating the image); and

decryption logic configured to decrypt the encrypted digital picture information received from the source device using a plurality of decryption keys (Par 003-006, 129, 143-150; plurality of decryption keys respective to each image tile/ pixel).

Alternatively, if the position of inherency is not found to be supportable, the examiner holds the position that it would have been obvious to a person with ordinary skill in the art to modify the Hayashi 's device by adding/ substituting Evans et al' s teachings of decryption logic configured to decrypt the encrypted digital picture information received from the source device using a plurality of decryption keys (Fig 11; Col 16, starts at line 10; per pixel encryption; plurality of encryption keys).

Regarding claim 30, Evans et al teaches the system wherein the source device is in communication with the receiving device through a network (Col 4, starts at line 56; network environment).

Regarding claim 36, Evans et al teaches the system wherein each source pixel includes a separate encryption logic embodied in a physical circuit that is connected to the source pixel (Col 3, line 45- Col 4, line 8; Col 12, starts at line 10; pixel element, and associated hardware elements).

Regarding claim 37, Evans et al teaches the system wherein each source pixel includes a separate encryption logic virtually connected to each of the source pixels through software programming in a communication device (Col 1, starts at line 40; Col 12, starts at line 5; drivers, hardware; and associated encryption logic/ software).

Regarding claim 41, Evans et al teaches the system wherein the communication device is a video card (Col 1, starts at line 40; Col 3, starts at line 13; video card).

Regarding claim 42, Evans et al teaches the system wherein the encryption logic is physical circuitry fabricated in a semi-conductor substrate and wherein the pixel elements are microelectronic devices (Col 5, starts at line 20; Col 12, starts at line 5; micro channel, micro processing devices; associated encryption logic/ software, and hardware).

Regarding claim 43, Hayashi teaches the system wherein the source device includes source pixel logic configured to access pixel information from the source pixels (Par 127-130, 139, 143, 149-150; receiving, outputting decryption logic/ information).

Regarding claim 44, Hayashi teaches the system wherein the source pixel logic identifies each region of source pixels and transmits captured digital picture information from each of the regions to the encryption logic (Fig 14; Par 006, 015, 040, 044, 150; communicating encryption keys/ information regarding stored image/ tiling groups).

Regarding claims 12, 31-35, 38-40 and 45-46, they recite the limitations of claims 9-11, 13-16, 29-30 and 41-44, therefore, they are rejected applying as above applied rejecting claims 9-11, 13-16, 29-30 and 41-44.

Conclusion

9. Examiner's note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may be applied as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention as well as the context of the passage as taught by the prior art or disclosed by the Examiner. Finally, for any future amendments to claims, the applicant is respectfully requested to incorporate the paragraph numbers from the specification upon which the support for such amendments were obtained.

10. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shanto M Z Abedin whose telephone number is 571-272-3551. The examiner can normally be reached on M-F from 10:30 AM to 7:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Moazzami Nasser, can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. The RightFax number for faxing directly to the examiner is 571-273-3551.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shanto M Z Abedin

Examiner, AU 2436

/Carl Colin/

Primary Examiner, Art Unit 2436